AMENDMENTS TO THE CLAIMS

Kindly amend claims 1, 9, and 14 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1.   (Currently Amended) An apparatus within a microprocessor, for managing power consumption of the microprocessor, said apparatus comprising:

a plurality of functional units each including a corresponding plurality of activity outputs, for indicating when a respective functional unit is enabled, wherein the value of each of said corresponding plurality of activity outputs indicates how much power, in Watts said respective functional unit is consuming;

utilization assessment logic, coupled to said plurality of activity outputs, for assessing activity thereof to determine a current total power consumption value, in Watts for the microprocessor;

power control logic, coupled to said utilization assessment logic, for comparing said current total power consumption value with a threshold power value, in Watts included in a specified power profile, wherein a select signal directs said power control logic to select said specified power profile from a plurality of power profiles that are stored within said power control logic; and

a power consumption controller, coupled to said power management logic and said plurality of functional units, for engaging one of a plurality of power reduction modes if said current total power consumption value exceeds said threshold power value.

2.   (Original) The apparatus as recited in claim 1, wherein one of said plurality of functional units is a cache and one of said plurality of power reduction modes is disabling said cache.

3.   (Original) The apparatus as recited in claim 1, wherein one of said plurality of functional units is a branch prediction unit and one of said plurality of power reduction modes is disabling said branch prediction unit.

4.   (Original) The apparatus as recited in claim 1, wherein one of said plurality of functional units is a floating point unit and one of said plurality of power reduction modes is disabling said floating point unit.

5.   (Original) The apparatus as recited in claim 1, wherein one of said plurality of functional units is an MMX unit and one of said plurality of power reduction modes is disabling said MMX unit.

6.   (Original) The apparatus as recited in claim 1, wherein one of said plurality of functional units is an execute unit and one of said plurality of power reduction modes is controlling power consumption of said execute unit by reducing a rate of issue of instructions to said execute unit.

7.   (Original) The apparatus as recited in claim 1, further comprising a clock of predetermined frequency coupled to said plurality of functional units, wherein one of said plurality of power reduction modes comprises reducing the frequency of said clock.

8.   (Original) The apparatus as recited in claim 1, further comprising a power supply voltage controller for controlling a supply voltage applied to said plurality of functional units, wherein one of said plurality of power reduction modes comprises reducing said supply voltage.

9.   (Currently Amended) A microprocessor power management mechanism within a microprocessor, comprising:

a plurality of functional units, each including an activity output for indicating when a respective functional unit is enabled, wherein the value ~~said activity~~of said activity output indicates how much power, in Watts, said respective functional unit is consuming;

power management logic, coupled to said activity outputs of the functional units,

for assessing the activity of individual functional units to determine a

current total power consumption value, in Watts, for the microprocessor;

and

a power consumption controller, coupled to said power management logic and

said plurality of functional units, for disabling or reducing the power

consumption of at least one of said plurality of functional units, if said

current total power consumption value exceeds a threshold power value, in

Watts, and wherein said threshold power value corresponds to one of a

plurality of power profiles stored within said power consumption

controller, and wherein a select signal directs said power consumption

controller to select said one of a plurality of power profiles.

10.   (Original) The microprocessor power management mechanism as recited in claim
9, further comprising a control bus coupled between said power management
logic and said power consumption controller.

11.   (Original) The microprocessor power management mechanism as recited in claim
10, wherein said power control logic sends a command over said control bus to
instruct said power consumption controller to disable a first one of said plurality
of functional units if said current total power consumption value exceeds said
threshold power value.

12.   (Original) The microprocessor power management mechanism as recited in claim
10, wherein said power control logic sends a command over said control bus to
instruct said power consumption controller to disable more than one of said
plurality of functional units if said current total power consumption value exceeds
said threshold power value.

13.   (Original) The processor of claim 10 wherein said power management logic comprises:

utilization assessment logic, for processing activity output signals from said respective activity outputs to determine said current total power consumption value.

14.   (Currently Amended) A method for managing power consumption in a microprocessor, the microprocessor including a plurality of functional units, the method comprising:

prescribing a plurality of power profiles for the microprocessor, the power profiles having corresponding threshold power values, in Watts;

storing the plurality of power profiles within the microprocessor;

selecting one of the plurality of power profiles and a corresponding selected threshold power value;

via the value of a corresponding activity signal, dynamically indicating how much power, in Watts, each of the individual functional units is consuming;

assessing activity of the individual functional units to determine a current total power consumption value, in Watts, for the microprocessor;

comparing the current total power consumption value with the selected threshold power value; and

if the current total power consumption value exceeds the selected threshold power value, engaging one of a plurality of power reduction modes.

15.   (Original) The method as recited in claim 14, wherein one of the plurality of power reduction modes includes disabling a first functional unit, the first functional unit being one of the plurality of functional units.

16.   (Original) The method as recited in claim 15, wherein the first functional unit is a cache.

17. (Original) The method as recited in claim 15 wherein the first functional unit is a branch prediction unit.

18. (Original) The method as recited in claim 15, wherein the first functional unit is a floating point unit.

19. (Original) The method as recited in claim 15, wherein the first functional unit is an MMX unit.

20. (Original) The method as recited in claim 14, wherein said engaging comprises:

    reducing a rate of issue of instructions to one or more of the plurality of functional
    units.

21. (Original) The method as recited in claim 14 wherein said engaging comprises:

    reducing the frequency of a core clock within the microprocessor.

22. (Original) The method of claim 14, wherein said engaging comprises:

    reducing an internal supply voltage from a first voltage to a second voltage.